REMARKS

In response to the Office Action mailed September 23, 2005, Applicant respectfully requests reconsideration.

Claims 1-6 were previously pending in this application. By this amendment, Applicant amends claims 1, 2 and 5 solely for clarification and adds claims 7-19. As a result, claims 1-19 are pending for examination, of which claims 1, 7 and 12 are independent. No new matter has been added.

1. Claims 1-6 Patentably Distinguish Over Hollander

Claim 1 stands rejected under 35 USC§ 102(e) as purportedly being anticipated by U.S. Patent No. 6,675,138 (Hollander). Applicant respectfully disagrees.

Hollander is directed to a system and method for detecting and measuring coverage of a functional verification programming environment during test generation over time as simulation is performed (col. 1, lines 7-12). The quality of a simulation model for the DUT is tested through temporal coverage of the testing and verification process (col. 4, lines 39-41). Temporal coverage examines the behavior of selected variables over time, according to a triggering event. Such a triggering event could be determined according to fixed, predefined sampling times and/or according to the occurrence of a temporal pattern of state transitions as defined by temporal expression given in a temporal language. This information is collected during the testing/verification process, and is then analyzed in order to determine the behavior of these variables (col. 4, lines 42-51).

Significantly, the term "state" is used in Hollander to denote the value of a single variable. Further, as is made clear throughout Hollander, the temporal coverage information is analyzed and searched for a coverage hole, indicated by the absence of a particular value from a family of values (col. 4, lines 51-54: col. 5, lines 2-5 and 14-17).

In contrast, claim 1 recites:

> A method of verifying a digital hardware design simulated in a hardware design language (HDL), including the steps of:
>
> defining at least one state to be verified, the at least one state including a set of signal values, each signal value corresponding to a respective one of a plurality of components within the hardware design;
>
> applying a test to the hardware design;

generating traces of internal signals within the hardware design during the test, each trace including signal data, time data and internal signal values associated with a respective one of the plurality of components; and

processing the traces to ascertain whether the plurality of components simultaneously had the signal values defined for the at least one state, thereby to ascertain whether the at least one state was achieved.

Hollander does not teach or suggest the step of "processing the traces to ascertain whether the plurality of components simultaneously had the signal values defined for the at least one state, thereby to ascertain whether the at least one state was achieved," as required by claim 1. Preliminarily, Hollander does not teach a "state" as this term is used in claim 1. As recited in claim 1, the at least one state includes a set of signal values, each signal value corresponding to a respective one of a plurality of components within the hardware design. In contrast, as noted above, Hollander uses the word "state" to denote the value of a *single variable*. Thus, rather than ascertaining whether a plurality of components within a hardware design simultaneously have the signal values defined for a *state*, as required by claim 1, Hollander describes determining the state of *individual variables* and ascertaining their presence or absence. That is, Hollander is specifically looking for a "coverage hole," indicated by the absence of a particular value from a family of values.

In view of the foregoing, Applicant respectfully submits that claim 1 patentably distinguishes over Hollander. Accordingly, Applicant respectfully requests that the rejection of claim 1 under §102(e) be withdrawn. Claims 2-6 each depend from claim 1 and are patentable for at least the same reasons. Accordingly, Applicant respectfully requests that the rejections of these claims be withdrawn.

2. New Claims 7-11 Patentably Distinguish Over Hollander

For reasons that should be clear from the discussion of Hollander set forth above, new claim 7 patentably distinguishes over Hollander at least because Hollander does not disclose or suggest the step of "processing the traces to ascertain whether the plurality of components simultaneously had the signal values defined for the at least one state, thereby to ascertain whether the at least one state was achieved," as recited in claim 1. Further, Hollander does not disclose or suggest the step of "pre-processing the traces such that, for at least each of the

components for which a signal value is defined within the at least one state, the trace associated with the component includes a signal value for each time for which the traces are to be processed." Claims 8-11 each depend from claim 7 and are patentable over Hollander for at least the same reasons.

3. New Claims 12-19 Patentably Distinguish Over Hollander

For reasons that should be clear from the discussion of Hollander set forth above, new claim 12 patentably distinguishes over Hollander because Hollander does not disclose or suggest the step of "determining whether the at least one state was achieved, including comparing signal values within the traces to the set of signal values defined for the at least one state." Claims 13-19 each depend from claim 12 and are patentable over Hollander for at least the same reasons.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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